The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A data conversion system comprising:

a first node and a second node in which one of ~~a plurality of nodes~~ the first node and the second node on an IEEE1394 bus serves as a cycle master, the first node being configured to transmit[[s]] first data to the second node ~~from one of the plurality of nodes to another node of the plurality of nodes~~ at a transfer rate synchronized with a cycle start packet output from the cycle master, ~~and converts the data in the other node of the plurality of nodes, wherein a first node of the plurality of nodes comprises:~~ the second node being having a data conversion unit configured to synchronize second data generated by conversion of the first data in the second node with an external reference signal, the second node to out put the second data,

an external synchronizing signal receiver for receiving [[an]] the external reference signal provided on at least one of the first and second nodes, and

a synchronization adjustment unit for ~~controlling the~~ synchronizing a frequency of the cycle start packet output from the cycle master with a frequency of the external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using the external reference signal[[,]] ~~and linking the frequency of the cycle start packet with the frequency of the reference signal received by the external synchronizing signal receiver, and~~

~~said first node or a second node of the plurality of nodes comprises a data conversion unit for converting the data and outputting the converted data at an output rate synchronized with the reference signal~~.

2. (Currently Amended) The data conversion system according to claim 1, wherein

the ~~transmitted~~ first data and the ~~converted~~ second data are image data, and

the ~~transmitted image~~ first data is a video signal in DV format and the ~~converted image~~ second data is an analog video signal or SDI video signal.

3. (Previously Presented) The data conversion system according to claim 1, wherein the first node serves as cycle master for data transfer.

4. (Previously Presented) The data conversion system according to claim 1, wherein

the second node comprises a second synchronization adjustment unit,

the frequency of the cycle start packet is linked with the frequency of the reference signal by the synchronization adjustment unit of the node that serves as the cycle master.

5 - 7. (Cancelled)

8. (Currently Amended) A device configured to connect to an IEEE1394 bus to form one of a first node and a second node, in a data conversion system in which one of the first node and the second node serves as a cycle master, the first node being configured to transfer a first data to the second node in synchronism with ~~for transmitting~~ a cycle start

packet ~~serving as a~~ output from the cycle master on [[an]] the IEEE1394 bus, ~~receiving data transmitted from a~~ the second node being connected on the IEEE1394 bus and being configured to synchronize second data generated by conversion of the first data in the second node with an external reference signal and to output the second data, the device ~~at a transfer rate that is synchronized with a frequency of the cycle start packet, and converting the received data~~ comprising:

an external synchronizing signal receiver for receiving [[a]] the external reference signal;

~~a data conversion unit for converting the received data and outputting the converted data at an output rate synchronized with the frequency of the reference signal;~~ and

a synchronization adjustment unit for synchronizing a frequency of ~~controlling the frequency of~~ the cycle start packet output from the cycle master ~~and linking the~~ with a frequency of the ~~cycle start packet with the frequency~~ external reference signal received by the external synchronizing signal receiver, by carrying out feedback control of a clock source frequency of the cycle master using of the external reference signal.

9. (Currently Amended) The device according to claim 1, wherein

the ~~received~~ first data and the second data are [[is]] image data, and

the ~~received image~~ first data is a video signal in DV format and the second data ~~outputted~~ is an analog video signal or SDI video signal.

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (New) The data conversion system according to claim 1, wherein the first node is hardware comprising an 13940HCI compliant IEEE1394 interface for outputting a video signal in DV format as first data, and the second node is data conversion hardware for outputting an analog video signal or SDI video signal as second data.

14. (New) The data conversion system according to claim 1, wherein the second node comprises the external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

15. (New) The data conversion system according to claim 1, wherein the first node comprises the synchronization adjustment unit, the second node comprises the external synchronizing signal receiver and synchronization adjustment unit, and the cycle start packet frequency is synchronized with the frequency of the external reference signal received by the external synchronizing signal receiver by means of the synchronization adjustment unit of the node that serves as cycle master.

16. (New) The data conversion system according to claim 15, wherein when the first node serves as cycle master, the external reference signal received by the external synchronizing signal receiver of the second node is transmitted from the second node to the first node by asynchronous transfer of an IEEE 1394 interface.

17. (New) The data conversion system according to claim 15, comprising a dedicated synchronization signal line for transmitting the external reference signal received by the external synchronizing signal receiver of the second node from the second node to the first node when the first node serves as cycle master.

18. (New) The data conversion system according to claim 1, wherein the first node comprises the external synchronizing signal receiver and synchronization adjustment unit, and serves as cycle master for data transfer.

19. (New) The data conversion system according to claim 1, wherein one of the first node and the second node serves and the cycle master and the other of the first node and the second node includes the synchronization adjustment unit.